

TUESDAY, September 19, 2006						
TIME	ESSCIRC				ESSDERC	
8:30 - 8:40	Introduction					
8:40 - 9:00	Joint Plenary Session - K. McGoldrick					
9:00 - 9:20	Coffee Break					
9:20 - 9:50	ESSCIRC Plenary Session - S. Kang					
9:50 - 10:10					A2L-G	A2L-H
10:10 - 10:30					High Performance MOSFETs with Innovative SD	Transport & Noise
10:30 - 10:50						
10:50 - 11:10	A3L-C	A3L-D	A3L-E		A4L-J	A4L-H
11:10 - 11:30	Receivers & Synthesizers	Low Power & Variability Aware Circuits	Advanced Mixed-Signal Techniques		Advance Gate Stack	MEMS & Sensors
11:30 - 11:50						
11:50 - 12:10						
12:10 - 12:30	Lunch Break					
12:30 - 14:00	Lunch Break					
14:00 - 14:20	Joint Plenary Session - T. Kuroda					
14:20 - 14:40						
14:40 - 15:00	A6L-C	A6L-D	A6L-E	A6L-F	ESSDERC Plenary Session - G. Bourianoff	
15:00 - 15:20	RF Subsystems	Advanced Architectures & Building Blocks	Mixed Signal Circuits & Systems	Continuous Time Sigma Delta Modulators		
15:20 - 15:40	Coffee Break					
15:40 - 16:00	Coffee Break					
16:00 - 16:10	Coffee Break					
16:10 - 16:30	A9L-C	A9L-D	A9L-E	A9L-F	A8L-G	A8L-H
16:30 - 16:50	Filters I	Low-Power Techniques for SoC Integration	Sensor Interfaces	Ultra Wideband Circuits	CMOS with Novel Gate-Stack Solutions	Advanced Transport Models for Nanoscale Devices
16:50 - 17:10						
17:10 - 17:30						
17:30 - 17:50	A8L-J RF Passive Integration					

WEDNESDAY, September 20, 2006						
TIME	ESSCIRC				ESSDERC	
8:30 - 8:40	2005 Best Paper Award					
8:40 - 9:00	Joint Plenary Session - H. Baltes					
9:00 - 9:20	Coffee Break					
9:20 - 9:50	ESSCIRC Plenary Session - R. Castello					
9:50 - 10:10					B2L-G	B2L-H
10:10 - 10:30					Carbon Nanotubes	Novel Memory
10:30 - 10:50					B2L-J Emerging Devices & Circuits 1	
10:50 - 11:10	B3L-C	B3L-D	B3L-E		B4L-G	B4L-H
11:10 - 11:30	Transceivers, Transmitters & PA	Memory Circuits	Other Analog Circuits		High-K Dielectrics in NVM	Fluctuations and Variations
11:30 - 11:50						
11:50 - 12:10						
12:10 - 12:30	Lunch Break					
12:30 - 14:00	Lunch Break					
14:00 - 14:20	Joint Plenary Session - C. Nguyen					
14:20 - 14:40						
14:40 - 15:00	B6L-C	B6L-D	B6L-E	B6L-F	ESSDERC Plenary Session - M. Lundstrom	
15:00 - 15:20	Filters II	RF Building Blocks	Amplifiers	Noise Issues in Sensors		
15:20 - 15:40	Coffee Break					
15:40 - 16:00	Coffee Break					
16:00 - 16:10	Coffee Break					
16:10 - 16:30	B9L-C	B9L-D	B9L-E	B9L-F	B8L-G	B8L-H
16:30 - 16:50	RF Circuits Beyond 20 GHz	High-Speed Data Converter Techniques	Sensors with Local Processing	Emerging Devices & Circuits 2	High Voltage Devices	Innovative Injection & Transport Devices
16:50 - 17:10						
17:10 - 17:30						
17:30 - 17:50	B8L-J Compact Models & Applications					

THURSDAY, September 21, 2006						
TIME	ESSCIRC				ESSDERC	
8:30 - 8:40	ESSCIRC/ESSDERC 2007 Presentation					
8:40 - 9:00	Joint Plenary Session - K. Uchida					
9:00 - 9:20	Coffee Break					
9:20 - 9:50	ESSCIRC Plenary Session - A. Abidi					
9:50 - 10:10					C2L-G	C2L-H
10:10 - 10:30					Imagers & Light Emitting Devices	Process Integration
10:30 - 10:50					C2L-J Carrier Mobility in Multi-Gate Devices	
10:50 - 11:10	C3L-C	C3L-D			C4L-G	C4L-H
11:10 - 11:30	VCO	Clocking & High-speed Digital Interfaces			Innovative Multigate Devices	High-K & Low-K Dielectrics
11:30 - 11:50						
11:50 - 12:10						
12:10 - 12:30	Lunch Break					
12:30 - 14:00	Lunch Break					
14:00 - 14:20	Joint Plenary Session - G. Gielen					
14:20 - 14:40						
14:40 - 15:00	C6L-C	C6L-D	C6L-E	C6L-F	ESSDERC Plenary Session - R. Woltjer	
15:00 - 15:20	Advanced Communications Interfaces	Switched Capacitor ADCs	High Speed Circuits	Power Management		
15:20 - 15:40	Coffee Break					
15:40 - 16:00	Coffee Break					
16:00 - 16:10	Coffee Break					
16:10 - 16:30	C9L-C	C9L-D	C9L-E		C8L-G	C8L-H
16:30 - 16:50	Pipeline ADC	Time Correlated Imaging	High Voltage Circuits & Systems		DRAM & Flash Memory	Emerging Materials & Devices
16:50 - 17:10						
17:10 - 17:30						
17:30 - 17:50	C8L-J Modeling of Gate Stacks & Dielectrics					
17:50 - 18:00	Closing Session					