

CONFERENCE VENUE

Montreux is located on the north shore of scenic Lac Lemman (Lake Geneva), a vibrant, centrally located and easily accessible area that includes the cities of Geneva, Lausanne, Montreux and Vevey. The larger area of western and central Switzerland also incorporates the important cities of Neuchâtel and Berne. The entire region has a rich background as a cultural and commercial hub with international recognition, and very close links with the industrial centers in eastern France, northern Italy, and southern Germany. The Geneva International Airport provides easy access to the Montreux-Vevey area from all over the world, while efficient train service as well as scenic highways offer reliable links to all metropolitan centers in south-central Europe. There is also direct, fast and frequent train connection between Geneva International Airport (GVA) and Montreux; the travel time between Geneva and Montreux is about one hour.

Montreux Convention Center

Conveniently located on the shores of Lake Geneva, and within easy walking distance to most of the hotels in the area, the Montreux Convention and Exhibition Center offers two large conference halls, numerous rooms for parallel technical sessions, and extensive support facilities. Traditional home of the world-famous Montreux Jazz Festival, the convention center provides the ideal venue for the event.

Montreux will be your home port for journeys of discovery through the canton of Vaud, the Lake Geneva Region, nearby France, or places which are famous for their history, their picturesque sites, their food and wine, or all of these and more. A suggestion to start with: the vineyards east and west of Lausanne are traversed high and low by pleasant footpaths, and in many of the vintners' villages – especially at weekends – cellars for wine tasting are open to the public.

In the heart of the country you are quite likely to find a centuries-old castle or fortified village – see Oron or Gruyères, for example. Geneva and Berne are fascinating blends of old and new, while further afield, in Interlaken or Lucerne, Zermatt or Chamonix, nearly every street has a mountain view.



Château de Chillon, Montreux

CONTACT INFORMATION

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Final Call for Papers

ESSDERC 2006

36th European Solid-State Device Research Conference

18-22 September 2006
Montreux, Switzerland

Paper submission deadline: 7 April 2006
Electronic Submission

Organization committee at:



Technical co-sponsorship:



IEEE



www.essderc2006.com

ESSDERC 2006 and ESSCIRC 2006 are held jointly.

GENERAL SCOPE OF THE CONFERENCE

The main themes for original contributions to be submitted to ESSDERC 2006 include (but are not limited to) the following:

➤ **Advanced Devices**

CMOS and bipolar devices covering device physics; novel MOS device structures (multiple gate, vertical, 3-D integrated FET, ballistic); circuit and device co-optimization; ultimate CMOS scaling issues; high performance, low power, and analog/RF devices; SOI; SGOI; strained silicon and SiGe device; silicon and silicon germanium bipolar transistors; high speed Si devices.

➤ **IC Manufacturing**

Advances in integrated circuits technology; advanced/novel memory process integration; logic and mixed-mode IC manufacturing; processes for performance; high-speed logic; multifunction integrated circuits; integrated passives; low power, low noise, analog, RF and mixed signal ICs; IC manufacturing technology and methodology; process control, failure analysis and related modeling; front-end and back-end process modules for fabrication of CMOS, memory, and BiCMOS devices.

➤ **Telecommunication, High-Voltage and Power Devices**

RF CMOS; passives; antennas; HBT; Bipolar; BiCMOS; high-voltage, high power devices; high temperature operation; SiC devices; MOS controlled power devices (e.g. DMOS, IGBT); smart power devices and ICs; IC cooling; devices for optical communications; optical links and interconnects; compound semiconductors (GaAs, InP, GaN, SiC, alloys) and optoelectronic device applications.

➤ **Modeling and Simulation**

Numerical and analytical modeling of solid-state electronic and optoelectronic devices; physical and compact circuit models for devices and interconnects; numerical simulation and modeling of fabrication processes; electro-thermal modeling and simulation.

➤ **Characterization and Reliability**

New device characterization methods; parameter extraction; test structures and methodologies; noise; charge-pumping; gate dielectric and device reliability; reliability of advanced interconnects and electromigration; reliability issues for new materials and devices (reliability of high-k and low-k materials); hot carriers; NBTI; defect control; equipment issues; monitoring; metrology; impact of back-end processing on devices; ESD; EMI.

➤ **Memory and System-on-Chip Technologies**

Embedded and stand-alone memories; nonvolatile; DRAM; FeRAM; MRAM; phase change and nano-crystal memories; single and few electron memories; above-IC integration of various detectors, sensors and actuators; devices and their integration for imaging; CMOS imagers; CCD's; TFT's; organic, amorphous, and polycrystalline devices; vacuum microelectronics; bonding techniques; IC cooling, packaging issues.

➤ **Sensors, MEMS, Flexible Electronics and Bio-Electronics**

Detectors, sensors and micro electromechanical (MEM) devices; resonators (MEMS, FBAR, new architectures); MEMS switches and passives for RF applications; integrated sensors; micro-optical devices; micro-fluidic devices; energy scavenging devices and micro-power generators; design, fabrication, modeling, reliability and packaging of all sensors and MEMS categories; organic electronics; flexible substrate electronics; devices and technologies for lab-on-chip; bio-sensors for chemical, molecular and biological applications; bio-electronic circuits and applications.

➤ **Emerging Devices, Nanotechnology, Nanophotonics, Quantum / Spin Electronics**

New nanoelectronic devices including nanotubes and nanowires (CNTs, semiconductor, metallic and DNA-templated nanowires), quantum dots and molecular devices; single electronics (SET, SEM and hybrids); nanotechnology and nanomaterials; advanced characterization of nanoelectronic devices and nanomaterials; new integrated functionality and emerging circuit architectures in nanoelectronics, photonic band-gap structures and crystals, molecular, nano-scale optoelectronics, optical and wireless on-chip ultra-scaled interconnects; new non-charge-based devices; spintronic devices and circuit applications.

To further emphasize the interactions between the device and circuits communities especially in the domain of emerging technologies, the conference will offer for the first time a joint session.

Joint ESSDERC/ESSCIRC Session on:

➤ **Circuits and Devices Using Emerging Silicon Nanoelectronics**

New integrated functionality in circuits and applications using non-classical MOSFET and/or nanowires, nanotubes, quantum and spin devices. Includes topics from ESSDERC tracks Advanced Devices and Emerging Devices and Nanotechnology in their circuit design context.

ESSCIRC / ESSDERC JOINT PLENARY TALKS

ESSCIRC and ESSDERC will share Plenary Sessions where distinguished invited speakers will discuss issues of interest for the attendees of both Conferences.

- **Georges Gielen** (KU Leuven)
Design Methodologies and Tools for Circuit Design in CMOS Nanometer Technologies
- **Karl McGoldrick** (Polymer Vision)
Mobile Friendly Rollable Displays
- **Henry Baltes** (ETH Zürich)
From Microsystems To Biosystems
- **Roger T. Howe** (Stanford University)
Integrated MEMS Resonator Technologies
- **Ken Uchida** (Toshiba Advanced LSI Laboratory)
Single Electron Transistors and Circuits for Future Low Power LSI
- **Tadahiro Kuroda** (Keio University)
Low-Power Inter-Chip Wireless Communication

ESSDERC PLENARY TALKS

- **Mark Lundstrom** (Purdue University)
Nano-Transistors: A Bottom-Up View
- **Reinout Veltjer** (Philips Research)
An Industrial View on Compact Modeling
- **George Bourianoff** (Intel Corporation)
Options and Opportunities for Beyond CMOS Logic Technologies

PAPER SUBMISSIONS

The 2006 ESSDERC Conference will allow only electronic submission of the papers in PDF format. Prospective authors must submit their paper(s) via the conference website.

Papers must be submitted in the final format to be published in the Proceedings. They must not exceed four A4 pages with all illustrations and references included. The size of the PDF files submitted should not exceed 2 Mbytes. Manuscript guidelines (MS Word, LaTeX and PDF) as well as instructions on how to submit electronically are available on the conference website.

Conference Website

<http://www.essderc2006.com>

All paper submissions must be received by Friday, 7 April 2006, 18h00 GMT.

After selection of papers, the authors will be informed of the decision of the Technical Program Committee by e-mail at the beginning of June 2006. At the same time, the complete program will be published on the internet.

The working language of the conference is English, which must also be used for all presentations and printed material.

REVIEW PROCESS

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the-art
- Specific results and their impact

The degree to which the paper deals with the above issues is fundamental to a successful review and selection of the paper. The most frequent cause of rejection of submitted papers is a lack of new results. Only work that has not been previously published at the time of the Conference will be considered. Submission of a paper for review and subsequent acceptance is considered by the Committee as a commitment that the work will not be placed in the public domain prior to the Conference.

BEST PAPER AWARDS

Papers presented at the Conference will be considered for the Best Paper Award and for the best "Young Scientist" Paper Award. The selection will be based on the judgment of the Conference participants and the award delivery will take place at ESSDERC 2007.

SCHEDULE AT A GLANCE

Monday	18 September 2006	Tutorials / Registration
Tuesday	19 September 2006	Conference Opening Technical Sessions Welcome Reception
Wednesday	20 September 2006	Technical Sessions Conference Gala Dinner
Thursday	21 September 2006	Technical Sessions
Friday	22 September 2006	Workshops Excursions

KEY DATES

Submission deadline	7 April 2006
Notification of acceptance	1 June 2006
Advance registration deadline	15 July 2006

TUTORIALS AND WORKSHOPS

Tutorials will be organized on Monday, 18 September 2006, while Workshops will take place on Friday, 22 September 2006. Please consult the conference website for further details.